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Word-serial address-event transceiver layout compiler

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New tools allow designers to create a verified chip layout from a neural model in minutes.

Neuromorphic systems use multiple neuron arrays to implement large systems that are both modular and scalable. These arrays, which may be on separate chips, communicate with each other using the address-event representation (AER), where each neuron in an array is assigned a unique binary address that is encoded and transmitted to other arrays when it spikes.[1] To facilitate the design of these neuromorphic systems, our lab has designed software for automatic placement and routing of AER transceiver circuitry and neuron arrays, and for padframe generation, pad routing, and design verification.

Our layout compiler—ChipGen, implemented using Tanner Inc.'s L-Comp tool—is continually modified to incorporate the latest developments in AER communication. Several people, including Kwabena Boahen, Kareem Zaghloul, and Brian Taba, have contributed to its development over the years. In its present incarnation, ChipGen utilizes word-serial address events, where the transmitter encodes all of a row's events in a single burst: the row's address followed by a column address for each event.[2] Similarly, the receiver decodes the burst into a row-wide data-word that is written to the selected row.[3]

In addition to compiling AER transmitter and receiver circuitry, ChipGen provides the option to include a scanner for the continuous sensing of currents through a clock-driven multiplexor. A more sophisticated scanner that outputs signals to a standard VGA monitor[4] may also be selected, in lieu of the transmitter.

To use ChipGen, the designer must first create a metapixel, which ChipGen tiles to create a neuron array that will use AER to communicate with others within the larger neuromorphic system. The metapixel contains a user's custom-designed neural model as well as standard circuitry for AER communication. This neural model can range from a single spiking neuron to a complex arrangement of dendrites, somas, and both excitatory and inhibitory synapses. A multiplicity of neurons is supported by assigning more than one row or column per metapixel.

The final step in the chip-design process is layout verification. To this end, we have developed a netlist generator, NetGen, that creates a SPICE netlist of the chip. This can then be compared to a netlist extracted from the layout in a procedure known as LVS (layout versus schematic). Starting with the original version written by Kai Hynna a few years ago, NetGen also continues to evolve in step with ChipGen.

We compiled ChipGen into a dynamically-linked library (DLL): it is loaded as a user programmable interface (UPI) macro in Tanner's L-Edit Pro version 11.[5] Our cell library is currently laid out in MOSIS SCN_DEEP (deep submicron) rules. Taiwan Semiconductor Manufacturing Company's (TSMC) 0.25μm CMOS process is the most advanced technology we have used to fabricate chips so far. NetGen is implemented as a stand-alone windows executable program.

Using ChipGen and NetGen, the chip designer can take their neural model and create a verified chip layout within minutes. Both of these programs, in addition to our AER cell library, are freely available upon request. More information can be obtained from our website.[6] In the near future, we plan to host a hands-on workshop that will go through the process of chip layout and design verification.

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